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(54) **Antenna switching d vice.**

(57) An antenna switching device of the present invention includes: a transmitting terminal for receiving a transmitting signal; a first antenna terminal connected to a first antenna; a second antenna terminal connected to a second antenna; a receiving terminal for outputting receiving signals received at the first antenna terminal and the second antenna terminal; a selecting unit for selecting one mode among a first

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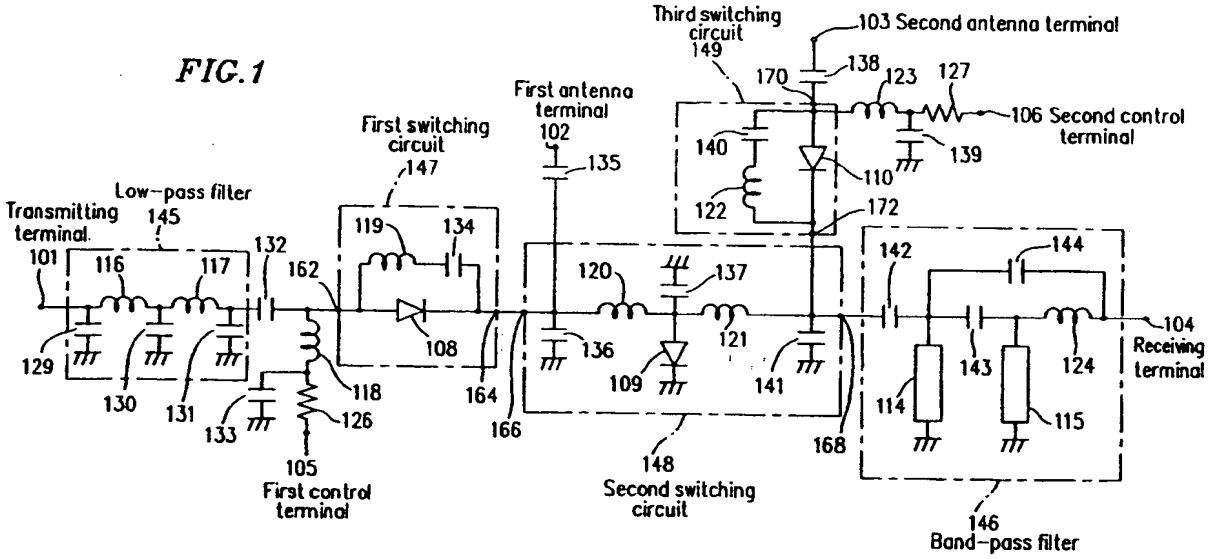
mode for outputting a signal corresponding to the transmitting signal to the first antenna terminal, a second mode for outputting the receiving signal received at the first antenna to the receiving terminal, and a third mode for outputting the receiving signal received at the second antenna to the receiving terminal.

*FIG. 1*



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# EUROPEAN SEARCH REPORT

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EP 94 11 3613

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int.Cl.6) |
|---|---|---|---|
| X | WO-A-85 00480 (MOTOROLA INC) 31 January 1985 | 1-3,6 | H04B1/48<br>H04B1/44 |
| A | * page 12, line 20 - line 36 *<br>* page 13, line 9 - line 14; figure 4 * | 10,11,28 | H04B7/08<br>H03K17/693<br>H01P1/15 |
| A | US-A-5 109 536 (KOMMRUSCH RICHARD S) 28 April 1992<br>* column 2, line 22 - line 35 *<br>* column 2, line 56 - line 61 *<br>* column 3, line 23 - line 35; figure 1 * | 1,7,19, 20,29 | |
| A | US-A-5 166 857 (AVANIC BRANKO ET AL) 24 November 1992<br>* column 6, line 59 - column 7, line 1; figure 5 * | 4,5, 21-26 | |
| A | EP-A-0 373 803 (RAYTHEON CO) 20 June 1990<br>* figures * | 14-18, 30-39 | |
| A | WO-A-90 06020 (MOTOROLA INC) 31 May 1990<br>* abstract *<br>* page 6, line 16 - line 35 *<br>* page 6, line 8 - line 10 *<br>* page 9, line 7 - line 19 * | 8,13,14, 21,22 | TECHNICAL FIELDS SEARCHED (Int.Cl.6)<br>H04B<br>H03K<br>H01P |
| A | 1988 IEEE MTT INTERNATIONAL MICROWAVE SYMPOSIUM DIGEST (CAT. NO.88CH2489-3), NEW YORK, NY, USA, 25-27 MAY 1988, 1988, NEW YORK, NY, USA, IEEE, USA, pages 371-374 vol.1, BRYANT D T 'A monolithic reduced-size Ku-band SPDT FET switch'<br>* page 371, left column, paragraph 2; figure 1 *<br>* page 372, left column, paragraph 2; figures 3,4 * | 8,9, 14-18 | |

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| THE HAGUE | 8 August 1995 | Goulding, C |

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
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## (54) High-frequency switch

(57) A high-frequency switch (10) is disclosed in which required resistors can be mounted without hampering the characteristics of the switch. The high-frequency switch (10) has a series circuit formed of a first diode (13a) and a first transmission line (14a). The first diode (13a) is connected to a transmitting circuit (Tx) through a capacitor. One end of the first transmission line (14a) is coupled to a receiving circuit (Rx) via a capacitor (12b). A second transmission line (14b) and a capacitor (12c) are connected between the node (A) and a ground potential, while a second diode (13b) and a capacitor (12d) are coupled between the node (B) and a ground potential. A series circuit formed of first and second resistors (15a, 15b) is connected between the nodes (C) and (D). A first control voltage terminal (Vc1) is coupl d to the node (C) via a resistor (16a), while a second control voltage terminal (Vc2) is connected to the node (D) via another resistor (16b). An antenna (ANT) and the node (E) are connected to the node (F).

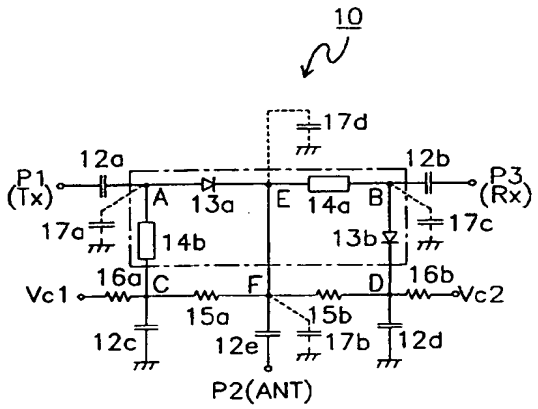


FIG. 1

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## Description

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

The present invention relates to a high-frequency switch and, more particularly, to a high-frequency switch for changing signal paths in a high-frequency circuit of, for example, a digital mobile cellular telephone.

#### 2. Description of the Related Art

A typical high-frequency switch is used in a digital mobile cellular telephone for connecting a second port (antenna ANT) either to a first port P1 (transmitting circuit Tx) or to a third port (receiving circuit Rx), as shown in Fig. 9.

Fig. 10 is a circuit diagram of one example of conventional high-frequency switches. In a high-frequency switch generally designated by 1, the first port P1 is connected to the transmitting circuit Tx; the second port P2 is coupled to the antenna ANT; and the third port P3 is connected to the receiving circuit Rx. Connected to the transmitting circuit Tx through a capacitor 2a is the anode of a first diode 3a which is grounded via a series circuit formed of a first transmission line 4a and a capacitor 2b. A first control voltage terminal 6a is connected across a resistor 5a to the node between the first transmission line 4a and the capacitor 2b. A first control circuit (not shown) for changing the switch 1 is connected to the first control voltage terminal 6a. The cathode of the first diode 3a is coupled to the antenna ANT through a capacitor 2c. A resistor 5b is further connected in parallel to the first diode 3a.

Moreover, a second transmission line 4b is connected at one end to the antenna ANT through the capacitor 2c and at the other end to the receiving circuit Rx through a capacitor 2d. The anode of a second diode 3b is coupled to the node between the second transmission line 4b and the capacitor 2d. The cathode of the second diode 3b is grounded via a capacitor 2e. A resistor 5c is connected in parallel to the second diode 3b. Moreover, a second control voltage terminal 6b is coupled across a resistor 5d to the node between the second diode 3b and the capacitor 2e. A second control circuit (not shown) for changing the high-frequency switch 1 is connected to the second control voltage terminal 6b.

An explanation will now be given of the transmitting and receiving operation performed by the high-frequency switch 1.

For transmission, a positive voltage is applied to the first control voltage terminal 6a, while 0 V is applied to the second control voltage terminal 6b. At this time, since the capacitors 2a through 2e interrupt the flow of a direct current, the voltage applied to the first control voltage terminal 6a is only applied to a circuit portion including the first and second diodes 3a and 3b. The first and second diodes 3a and 3b can thus be activated. This makes it possible to transmit a signal from the transmitting circuit Tx to the antenna ANT and then radiates from the antenna ANT. Further, an impedance inverting circuit is formed by causing the second transmission line 4b to be grounded via the second diode 3b and the capacitor 2e. Accordingly, the impedance viewed from the node between the cathode of the first diode 3a and the second transmission line 4b to the receiving circuit Rx is caused to become very large. As a result, the signal sent from the transmitting circuit Tx cannot be transmitted to the receiving circuit Rx.

Conversely, for reception 0 V is applied to the first control voltage terminal 6a, while a positive voltage is applied to the second control voltage terminal 6b, so that the first and second diodes 3a and 3b are rendered ineffectual. A receiving signal is thus transmitted to the receiving circuit Rx rather than to the transmitting circuit Tx. In this manner, transmission and reception can be changed in this high-frequency switch 1 by controlling the voltages to be applied to the first and second control voltage terminals 6a and 6b.

However, in this known type of the high-frequency switch 1, it is required that the resistors 5b and 5c be connected in parallel to the first and second diodes 3a and 3b, respectively, thereby restricting the flexibility of designing the switch 1. In particular, for forming the switch 1 by the use of a multilayered substrate, if the first and second diodes 3a and 3b are mounted on a multilayered substrate, the resistors 5b and 5c are also required to be mounted or printed on the substrate. This increases the manufacturing cost.

Additionally, if a multilayered substrate partly forming the switch 1 and the resistors 5b and 5c are mounted on a printed circuit board, wiring is required for the resistors 5b and 5c. This lowers the characteristics of the high-frequency switch 1, thereby failing to obtain desired characteristics.

### SUMMARY OF THE INVENTION

Acc rdingly, it is an object of the present invention to provide a high-frequency switch, free from the above-described problems, in which required resistors can be mounted on a printed circuit board without hampering the characteristics of the switch.

In order to achieve the above object, according to one aspect of the present invention, there is provided a high-frequ ncy switch having first through third ports so as to connect the second port either to the first port or to the third port,

the high-frequency switch comprising:

a series circuit formed of a first transmission line and a first diode which is connected between the first and third ports;

a second transmission line connected between a reference potential and the node of the first port and the first diode;

a second diode connected between a reference potential and the node of the third port and the first transmission line;

a series circuit formed of first and second resistors connected between the node of the second transmission line and the reference potential coupled to the second transmission line and the node of the second diode and the reference potential coupled to the second diode;

a first control voltage terminal connected to one end of the first resistor; and

a second control voltage terminal connected to one end of the second resistor, wherein the node between the second port, the first diode and the first transmission line is connected to the node between the first and second resistors.

According to another aspect of the present invention, there is provided a high-frequency switch having first through third ports so as to connect the second port either to the first port or to the third port, the high- frequency switch comprising:

a series circuit formed of a first transmission line and a first diode which is connected between the first and third ports;

a second transmission line connected between a reference potential and the node of the first port and the first diode;

a second diode connected between a reference potential and the node of the third port and the first transmission line;

a series circuit formed of first and second resistors connected between the node of the second transmission line and the reference potential coupled to the second transmission line and the node of the second diode and the reference potential coupled to the second diode;

a third transmission line connected between the node of the first diode and the first transmission line and the node of the first and second resistors; a first control voltage terminal connected to one end of the first resistor; and

a second control voltage terminal connected to one end of the second resistor, wherein the second port is connected to the node between the first diode and the first transmission line, and the node between the first and second resistors is connected to a reference potential.

In the above-described high-frequency switches, at least one of the first and second control voltage terminals may be coupled to one end of one of the first and second resistors via a resistor. Also, at least one of the first through third ports may be coupled to a reference potential via a capacitor.

The aforedescribed high-frequency switches may further comprise a third resistor connected to one end of the first resistor and the node between the second transmission line and a reference potential and a fourth resistor connected to one end of the second resistor and the node between the second diode and a reference potential.

Further, a series circuit formed of a transmission line and a capacitor may be connected in parallel to at least one of the first and second diodes. Alternatively, a series circuit formed of a transmission line and a capacitor may be connected in parallel to at least one of the first and second diodes, and another capacitor may be further connected in parallel to the above-mentioned series circuit.

With th above arrangements, a forward bias voltage is applied to the first and second diodes during transmission, thus causing the diodes to be activated. Accordingly, a signal from th transmitting circuit is transmitted to the antenna via the first diode and then radiates from the antenna. Also, an impedance inverting circuit can be formed by causing the first transmission line to be grounded via the second diode and the capacitor. Accordingly, the impedance viewed

from the antenna to the receiving circuit becomes vary large, and thus, a transmitting signal from the transmitting circuit is not sent to the receiving circuit. In contrast, during reception the first and second diodes are rendered ineffective, and thus, a receiving signal is transmitted to the receiving circuit rather than to the transmitting circuit.

## BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram of a first embodiment of a high-frequency switch according to the present invention;

Fig. 2 is a top view of the high-frequency switch shown in Fig. 1;

Fig. 3 is an exploded perspective view of a multilayered substrate used for the high-frequency switch shown in Fig. 1;

Fig. 4 is a circuit diagram of a second embodiment of a high-frequency switch according to the present invention;

Fig. 5 is a circuit diagram illustrating a second modification example of the high-frequency switch;

Fig. 6 is a circuit diagram illustrating a further example of a second modification example of the high-frequency switch;

Fig. 7 is a circuit diagram illustrating a third modification example of the high-frequency switch;

Fig. 8 is a circuit diagram illustrating a fourth modification example of the high-frequency switch;

Fig. 9 is a schematic diagram illustrating the operation of a high-frequency switch; and

Fig. 10 is a circuit diagram of a high-frequency switch of a known type.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will now be described with reference to the drawings. In the following description, the elements as the same as or corresponding to those of a first embodiment are designated by like reference numerals in the subsequent embodiments, and an explanation thereof will thus be omitted.

Fig. 1 is a circuit diagram of a first embodiment of a high-frequency switch according to the present invention. In a high-frequency switch generally indicated by 10, a first port P1 is connected to a transmitting circuit Tx; a second port P2 is coupled to an antenna ANT; and a third port P3 is connected to a receiving circuit Rx. The anode of a first diode 13a is coupled to the transmitting circuit Tx through a capacitor 12a. A first transmission line 14a is connected at one end to the cathode of the first diode 13a and at the other end to the receiving circuit Rx across a capacitor 12b.

Further, a second transmission line 14b is coupled at one end to the node A between the first diode 13a and the capacitor 12a and at the other end to a reference potential, i.e., a ground potential, via a capacitor 12c. Also, the anode of a second diode 13b is connected to the node B between the first transmission line 14a and the capacitor 12b, while the cathode of the second diode 13b is connected to a ground potential via a capacitor 12d.

Moreover, a series circuit formed of first and second resistors 15a and 15b is connected between the node C of the second transmission line 14b and the capacitor 12c and the node D of the second diode 13b and the capacitor 12d.

A first control voltage terminal Vc1 is coupled through a resistor 16a to the node C between the second transmission line 14b and the capacitor 12c. A first control circuit for changing the switch 10 (not shown) is further connected to the first control voltage terminal Vc1. Also, a second control voltage terminal Vc2 is coupled across a resistor 16b to the node D between the second diode 13b and the capacitor 12d. A second control circuit for changing the switch 1 (unillustrated) is connected to the second control voltage terminal Vc2.

The node F between the first and second resistors 15a and 15b is connected to the antenna ANT via a capacitor 12e. The nodes E and F are directly coupled to each other.

With the above-described arrangement, the first and second transmission lines 14a and 14b are formed of striplines, microstrip lines, coplanar guide lines, or the like, all of the lines having a wavelength shorter than $\lambda/4$ when the wavelength of a high-frequency signal transmitted to the switch 10 is represented by $\lambda$. The second transmission line 14b may be substituted with a high-impedance line.

Th first and second transmission lines 14a and 14b are what is referred to as "the $\lambda/4$ lines". In practice, however, the lines 14a and 14b are configured to have a wavelength shorter than $\lambda/4$, as discussed above, due to the floating capacitance and the inductance of the lines.

The operation of the high-frequency switch 10 constructed as described above will now be explained while referring

to Table 1 illustrating the control operation. In Table 1, "V1 and V2" designate control voltages to be applied to the first and second control voltage terminals Vc1 and Vc2 (+ indicates a positive control voltage, while 0 represents a ground voltage). "Tx-ANT" depicts the open/close state between the transmitting circuit port Tx and the antenna port ANT (o designates the connecting (close) state, while x indicates the open state). "ANT-Rx" represents the open/close state between the antenna port ANT and the receiving circuit port Rx (o designates the connecting (close) state, while x indicates the open state).

Table 1

| Connecting state | V1 | V2 | Tx-ANT | ANT-Rx |
|---|---|---|---|---|
| First | + | 0 | o | x |
| Second | 0 | + | x | o |

For transmission, a positive voltage is applied to the first control voltage terminal Vc1, while a ground potential, i.e., 0 V, is applied to the second control voltage terminal Vc2. At this time, the capacitors 12a through 12f interrupt the flow of a direct current, and thus, the voltage applied to the first control voltage terminal Vc1 is applied only to the circuit including the first and second diodes 13a and 13b. This causes the first and second diodes 13a and 13b to be activated. Simultaneously, a signal from the transmitting circuit Tx is transmitted to the antenna ANT and then radiates from the antenna ANT. Also, an impedance inverting circuit is formed by causing the first transmission line 14a to be grounded via the second diode 13b and the capacitor 12d. Accordingly, the impedance viewed from the node E between the cathode of the first diode 13a and the first transmission line 14a to the receiving circuit Rx is caused to become very large. As a result, the transmitting signal from the transmitting circuit Tx is not sent to the receiving circuit Rx.

Conversely, for reception 0 V is applied to the first control voltage terminal Vc1, while a positive voltage is applied to the second control voltage terminal Vc2, so as to cause the first and second diodes 13a and 13b to be ineffective. A receiving signal is thus transmitted to the receiving circuit Rx rather than to the transmitting circuit Tx. It should be noted that the first and second resistors 15a and 15b are provided for stabilizing the capacitances produced by reverse-biasing the first and second diodes 13a and 13b, respectively, during reception.

In this manner, voltages to be applied to the first and second voltage terminals Vc1 and Vc2 can be regulated, thereby changing between the transmitting and receiving operation performed by this switch 10.

Fig. 2 is a top view of the high-frequency switch 10. In this switch 10, mounted on a circuit board 22 are a multilayered substrate 21 into which a portion defined by a one-dot-chain line shown in Fig. 1 is integrated, the capacitors 12a through 12e, and the first and second resistors 15a and 15b.

This multilayered substrate 21 is formed, as shown in Fig. 3, by stacking a plurality of dielectric layers 23a through 23d. Formed on the dielectric layer 23a, which is the uppermost layer, are four lands 24a through 24d. The first diode 13a is mounted on the lands 24a and 24b, while the second diode 13b is mounted on the lands 24c and 24d. A first ground electrode 25a is disposed on the dielectric layer 23b, which is the second layer from the top. Further, the first transmission lines 14a and 14b are formed on the dielectric layer 23c, which is the third layer from the top, and a second ground electrode 25b is disposed on the dielectric layer 23d, which is the lowermost layer.

With this arrangement, the anode of the first diode 13a is connected to one end of the second transmission line 14b through the land 24a formed on the dielectric layer 23a and via holes formed in the dielectric layers 23a and 23b. The cathode of the first diode 13a is coupled to one end of the first transmission line 14a through the land 24b formed on the dielectric layer 23a and via holes formed in the dielectric layers 23a and 23b. In contrast, the anode of the second diode 13b is connected to the other end of the first transmission line 14a through the land 24c formed on the dielectric layer 23a and via holes formed in the dielectric layers 23a and 23b.

Disposed on the top surface and the lateral surfaces of the substrate 21 are, as illustrated in Fig. 2, eight external electrodes 26a through 26h. Moreover, lands 27a through 27e to be connected to the external electrodes 26a through 26h are formed on the mounting board 22.

Among the external electrodes 26a through 26h, the electrode 26a is coupled to one end of the second transmission line 14b and is further connected to the transmitting circuit Tx through the land 27a and the capacitor 12a. Also, the external electrode 26b is coupled to a ground GND as a ground terminal. The electrode 26c is connected to the other end of the first transmission line 14a and is further coupled to the receiving circuit Rx across the land 27c and the capacitor 12b. Moreover, the electrodes 26d and 26h are connected to the first and second ground electrodes 25a and 25b, respectively, and are coupled to GNDs as ground terminals. Further, the electrode 26e is connected to the cathode of the second diode 13b and is further coupled to a GND via the land 27c and the capacitor 12d. The electrode 26e is then used as the second control voltage terminal Vc2 through the land 27d and the resistor 16b. The electrode 26f is connected to one end of the first transmission line 14a and is further coupled to the antenna ANT through the land 27a

and the capacitor 12e. Further, the electrode 26g is connected to the other end of the second transmission line 14b and is further coupled to a GND via the land 27e and the capacitor 12c. The electrode 26g is then used as the first control voltage terminal Vc1 through the land 27f and the resistor 16a. The resistor 15a is connected between the lands 27d and 27e, while the resistor 15b is coupled between the lands 27c and 27d.

According to the aforedescribed construction, the high-frequency switch 10 having the circuit shown in Fig. 1 can be formed.

Fig. 4 is a circuit diagram of a second embodiment of a high-frequency switch according to the present invention. A high-frequency switch generally designated by 20 is different from the high-frequency switch 10 of the first embodiment in the following points. The antenna ANT is connected through the capacitor 12e to the node E between the first diode 13a and the first transmission line 14a; the node F between the first and second resistors 15a and 15b is coupled to a ground potential via a capacitor 12f; and a third transmission line 14c is connected between the nodes E and F.

With this construction, the first through third transmission lines 14a through 14c are formed of striplines, microstrip lines, coplanar guide lines, or the like, all of the lines having a wavelength shorter than $\lambda/4$ when the wavelength of a high-frequency signal supplied to the high-frequency switch 20 is represented by $\lambda$. The second and third transmission lines 14b and 14c may be substituted with high-impedance lines. The first through third transmission lines 14a through 14c are what is referred to as "the $\lambda/4$ lines". In practice, however, the lines 14a through 14c are configured to have a wavelength shorter than $\lambda/4$, as described above, due to the floating capacitance and the inductance of the lines.

The operation of the high-frequency switch 20 constructed as described above is similar to that of the switch 10 indicated by Table 1.

According to the above description, in the high- frequency switches 10 and 20 of the first and second embodiments, it is possible to dispose resistors at positions away from the diodes, unlike a conventional type of high-frequency switches in which resistors are required to be connected in parallel to the diodes. This increases the flexibility of designing the circuit configuration. Also, resistors can be separated from the signal paths so as to increase the Q factor, thereby lowering insertion losses of the high-frequency switches. Further, resistors can be directly mounted on a circuit board without having to be mounted on or integrated into a multilayered substrate, thereby decreasing the cost and size of the substrate. Additionally, the elements other than the resistors forming the switches can be completely or partly mounted on or integrated into the substrate, thereby enabling a decrease in the cost and size of the substrate.

In this invention, a ground potential may be applied instead of a positive control voltage, and a negative control voltage may be applied in place of a ground potential. In this case, in the above-described first connecting state shown in Table 1, a ground potential, i.e., 0 V, is applied to the first control voltage terminal Vc1, while a negative control voltage is applied to the second control voltage terminal Vc2. The same applies to the implementation of the second connecting state.

The directions of the first and second diodes 13a and 13b are not limited to those of the first and second embodiments illustrated in Figs. 1 and 4. They may be reversely connected. More specifically, the first diode 13a may be connected at its anode to the first transmission line 14a and at its cathode to the capacitor 12a. The second diode 13b may be coupled at its anode to the capacitor 12d and at its cathode to the first transmission line 14a. In this case, since the polarities of the first and second diodes 13a and 13b are reversed, it is also required that a positive control voltage and a ground potential to be applied to the first and second control voltage terminals be reversed to Table 1.

Moreover, the resistors 16a and 16b are provided to adjust the control voltages to be applied to the switch via the nodes C and D from the first and second control voltage terminals Vc1 and Vc2, respectively. Thus, the resistors 16a and 16b may be omitted as required, in which case, the nodes C and D may be directly connected to the first and second control voltage terminals Vc1 and Vc2, respectively. Additionally, the capacitors 12a through 12f, which serve to eliminate bias voltages, may be omitted as required.

An explanation will now be given of a first modification example of the high-frequency switches 10 and 20. As indicated by the broken lines of Figs. 1 and 4, capacitors 17a through 17d may be preferably connected between the first through the third ports P1 through P3 and reference potentials, respectively. In this case, the capacitances of the capacitors 17a through 17d can be determined to correct the characteristic impedance, thereby effectively reducing insertion losses and reflection losses of the high-frequency switches 10 and 20. Additionally, the first through third transmission lines 14a through 14c can be shortened, thereby enhancing the downsizing of the switches 10 and 20. All of the capacitors 17a through 17d are not necessarily used, and only some of them may be connected to the corresponding portions of the switches 10 and 20 as required.

A description will further be given of a second modification example of the high-frequency switches 10 and 20 while referring to Fig. 5. More preferably, a series circuit formed of the first and third resistors 15a and 15c may be connected between the nodes C and F, while a series circuit formed of the second and fourth resistors 15b and 15d may be coupled between the nodes D and F. Then, the first control voltage terminal Vc1 may be connected via the resistor 16a to the node G between the first and third resistors 15a and 15c, while the second control voltage terminal Vc2 may be coupled through the resistor 16b to the node H between the second and fourth resistors 15b and 15d. With this configuration, the third and fourth resistors 15c and 15d specify the voltages to be applied to the first and second diodes 13a and 13b, respectively, during transmission, so as to stabilize the capacitance generated by reverse-biasing.

To further develop the second modification example, another example is shown in Fig. 6. In this example, the first control voltage terminal Vc1 may be connected to the node G through the resistor 16a, while the second control voltage terminal Vc2 may be coupled to the node D across the resistor 16b. In this example, advantages similar to those achieved by the second modification example illustrated in Fig. 5 can also be obtained. It should be noted that the first control voltage terminal Vc1 may be connected to the node C and the second control voltage terminal Vc2 may be coupled to the node H. In this case, advantages similar to those realized by the second modification example shown in Fig. 5 can be obtained.

An explanation will further be given of third and fourth modification examples of the high-frequency switches 10 and 20 while referring to Figs. 7 and 8. In these examples, the below-described circuit devices may be connected either to the first diode 13a or to the second diode 13b. An explanation will be given of the examples in which the devices are provided for the first diode 13a by way of example while referring to Figs. 7 and 8.

In the third modification example, as illustrated in Fig. 7, a series circuit formed of a transmission line 18 and a capacitor 19a may be coupled in parallel to the first diode 13a. With this arrangement, a parallel resonance circuit can be form d by a capacitance of the inactivated first diode 13a and an inductance of the transmission line 18. Accordingly, the inductance of the transmission line 18 can be determined to match the resonant frequency of the parallel resonance circuit to the frequency of a high-frequency signal to be transmitted to the switch 10 or 20, thereby enhancing the impedance of the first diode 13a in the inactivated state. As a consequence, the isolation characteristics of the first diode 13a in the inactivated state can be improved. The capacitor 19a is provided for preventing the bypassing of a direct current flowing via the transmission line 18.

The transmission line 18 is formed of a stripline, a microstrip line, a coplanar guide line or the like, and the length and impedance of the line 18 are determined so that the resonant frequency of the parallel resonance circuit can match the frequency of a high-frequency signal. The transmission line 18 may be substituted with a high-impedance line.

To further develop the third modification example, the fourth example is provided. That is, if the capacitance of the first diode 13a is too small to obtain a desired resonant frequency, a capacitor 19b is coupled, as illustrated in Fig. 8, in parallel to a series circuit formed of the transmission line 18 and the capacitor 19a connected to the first diode 13a. With this configuration, a parallel resonance circuit can be formed by the synthetic capacitance of the inactivated first diode 13a and the capacitor 19b and an inductance of the transmission line 18a, thereby obtaining a desired resonant frequency.

It should be noted that the first through fourth modification examples may be combined with each other.

As will be clearly understood from the foregoing description, the high-frequency switch of the present invention offers the following advantages.

Resistors can be disposed at the positions away from the diodes, unlike the conventional type of high-frequency switches in which resistors are required to be connected in parallel to the diodes. Hence, the flexibility of designing the circuit configuration can be increased. Also, the resistors can be separated from the signal paths so as to increase the Q factor, thereby lowering the insertion losses of the switch. Further, resistors can be mounted on a circuit board without needing to mount on or integrated into a multilayered substrate, thereby decreasing the cost and size of the substrate. Additionally, the elements other than the resistors constituting the switch can be completely or partly mounted on or integrated into a multilayered substrate, thereby enabling a decrease in the cost and size of the substrate.

If an additional resistor is connected to each of the first and second control voltage terminals, the resistance of the resistor can be determined to readily adjust the control voltages and the control currents at the first and second control voltage terminals.

Further, if a capacitor is connected between each of the first through third ports and a reference potential, the capacitance of the capacitor can be selected to correct the characteristic impedance. This can effectively reduce insertion losses and reflection losses of the switch. Additionally, the first through third transmission lines can be shortened, thereby enhancing the downsizing of the high-frequency switch.

If third and fourth resistors are added to the first and second resistors, they can specify voltages to be applied to the first and second diodes during transmission, and thus stabilize the capacitance produced by reverse biasing.

If a series circuit formed of a transmission line and a capacitor is connected in parallel to one of the first and second diodes, a parallel resonance circuit can be formed by a capacitance of the diode in the disenergized state and an inductance of the transmission line. The inductance of the line can be determined to match the resonant frequency of the parallel resonance circuit to the frequency of a high-frequency signal to be transmitted to the switch, thereby improving the impedance of the diode when it is disenergized. As a consequence, isolation characteristics can be enhanced. Additionally, the capacitor connected in series to the transmission line can avoid the bypassing of a direct current flowing into a circuit portion including the transmission line.

If an extra capacitor is connected in parallel t the above-described series circuit formed of the transmission line and the capacitor coupled to one of the first and second diodes, a parallel resonance circuit can be formed by the synthetic capacitance of the inactivated diode and the capacitor connected in parallel t the diode and the inductance of the transmission line. It is thus possible to achieve a desired resonant frequency and to also improve the isolation characteristics.

## Claims

1. A high-frequency switch (10) having first through third ports (P1, P2, P3) wherein the second port (P2) can be connected either to the first port (P1) or to the third port (P3), said high-frequency switch (10) comprising:

   a series circuit formed of a first transmission line (14a) and a first diode (13a) which is connected between the first and third ports (P1, P3);

   a second transmission line (14b) connected between a reference potential and a node (A) between the first port (P1) and said first diode (13a);

   a second diode (13b) connected between a reference potential and a node (B) between the third port (P3) and said first transmission line (14a);

   a series circuit formed of first and second resistors (15a, 15b) connected between a node (C) between said second transmission line (14b) and the reference potential, and a node (D) between said second diode (13b) and the reference potential;

   a first control voltage terminal (Vc1) connected to one end of said first resistor (15a); and

   a second control voltage terminal (Vc2) connected to one end of said second resistor (15b),

   wherein a node (E) between said first diode (13a) and said first transmission line (14a) is connected to a node (F) between said first and second resistors (15a, 15b) and to said second port P2.

2. A high-frequency switch (20) having first through third ports (P1, P2, P3) wherein the second port (P2) can be connected either to the first port (P1) or to the third port (P3), said high-frequency switch comprising:

   a series circuit formed of a first transmission line (14a) and a first diode (13a) which is connected between the first and third ports (P1, P3);

   a second transmission line (14b) connected between a reference potential and a node (A) between the first port (P1) and said first diode (13a);

   a second diode (13b) connected between a reference potential and a node (A) between the third port (P3) and said first transmission line (14a);

   a series circuit formed of first and second resistors (15a, 15b) connected between a node (C) between said second transmission line (14b) and the reference potential, and a node (D) between said second diode (13b) and the reference potential;

   a third transmission line (14c) connected between a node (E) between said first diode (13a) and said first transmission line (14a) and a node (F) between said first and second resistors (15a, 15b);

   a first control voltage terminal (Vc1) connected to one end of said first resistor (15a); and

   a second control voltage terminal (Vc2) connected to one end of said second resistor (15b),

   wherein said second port (P2) is connected to the node (E) between said first diode (13a) and said first transmission line (14a), and a node (F) between said first and second resistors (15a, 15b) is connected to a reference potential.

3. A high-frequency switch (10; 20) according to claim 1 or 2, wherein at least one of said first and second control voltage terminals (Vc1, Vc2) is coupled to the corresponding end of said one of said first and second resistors (15a, 15b) via an additional resistor (16a, 16b).

4. A high-frequency switch (10; 20) according to any of the claims 1 to 3, further comprising a third resistor connected to said one end of said first resistor (15a) and said node (C) between said second transmission line and a reference potential, and a fourth resistor connected to said one end of said second resistor (15b) and said node (D) between

said second diode (13b) and a reference potential.

5. A high-frequency switch (10; 20) according to any of the claims 1 through 4, wherein at least one of the first through third ports (P1, P2, P3) is coupled to a reference potential via a capacitor (17a, 17b, 17c).

6. A high-frequency switch (10; 20) according to any of the claims 1 to 5, wherein a series circuit of a transmission line (18) and a capacitor (19a) is connected in parallel with at least one of said first and second diodes (13a, 13b).

7. A high-frequency switch (10) according to any of the claims 1 to 5, wherein a series circuit formed of a transmission line (18) and a capacitor (19a) is connected in parallel to at least one of said first and second diodes (13a, 13b), and another capacitor (19b) is further connected in parallel to said series circuit.

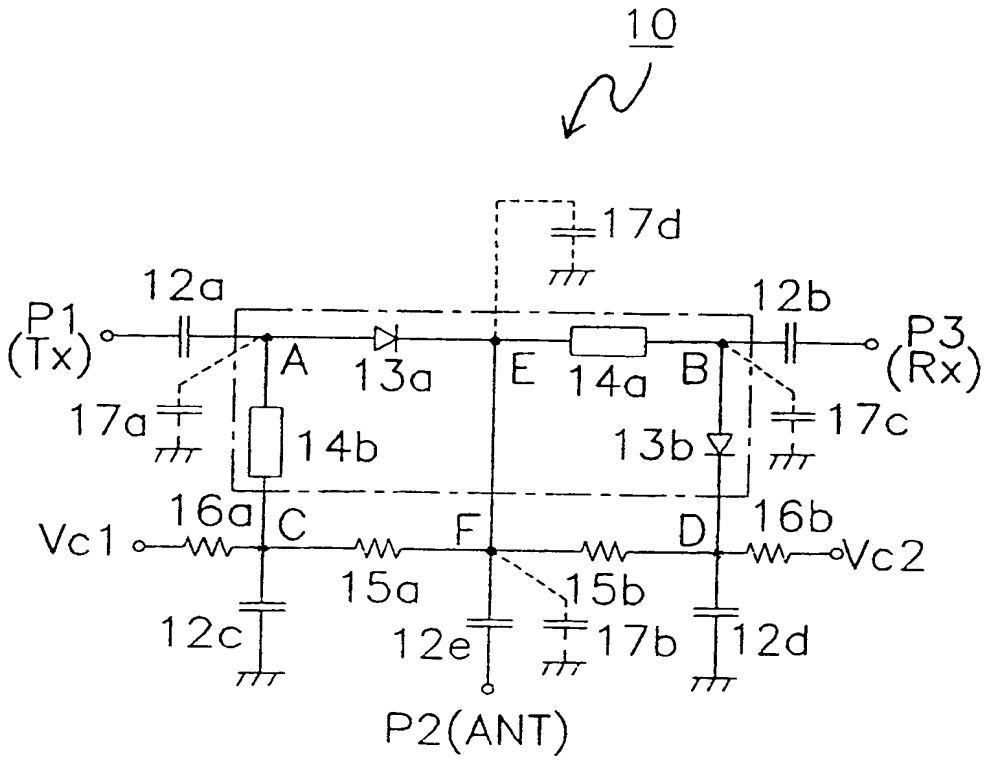


FIG. 1

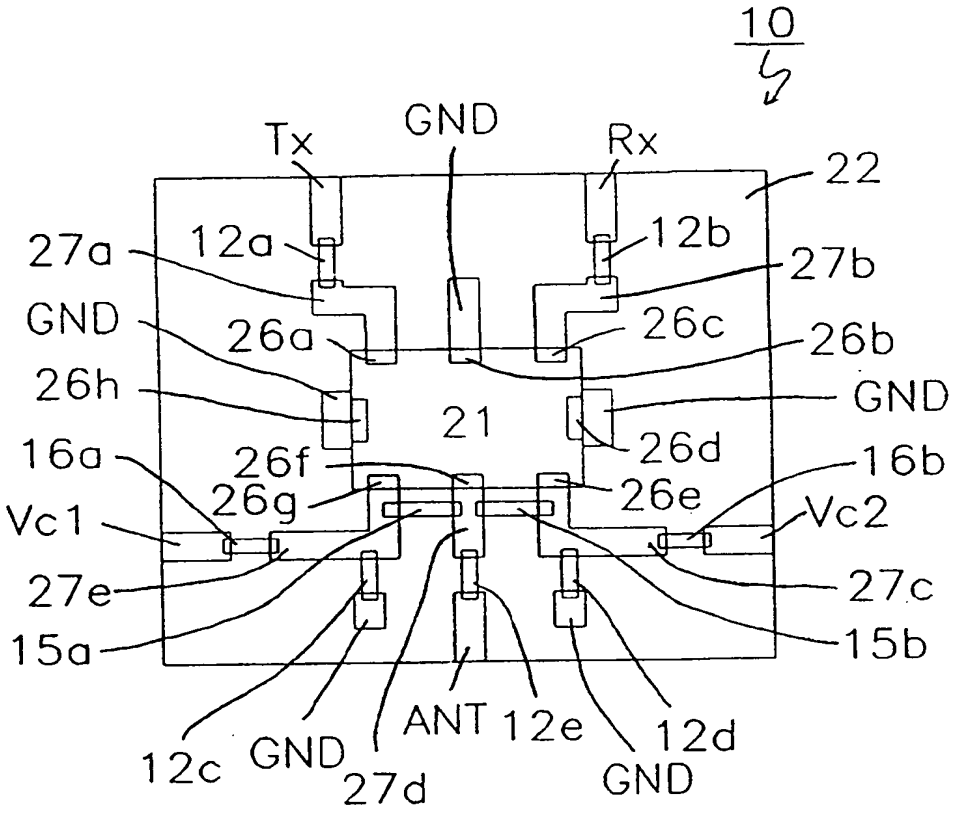


FIG. 2

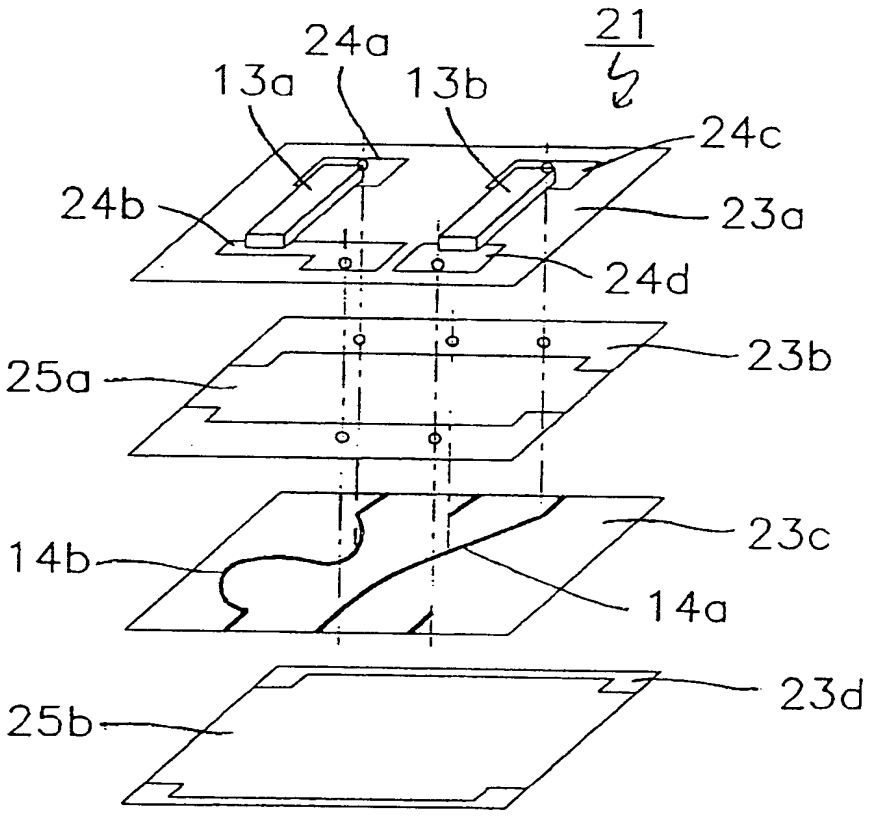


FIG. 3

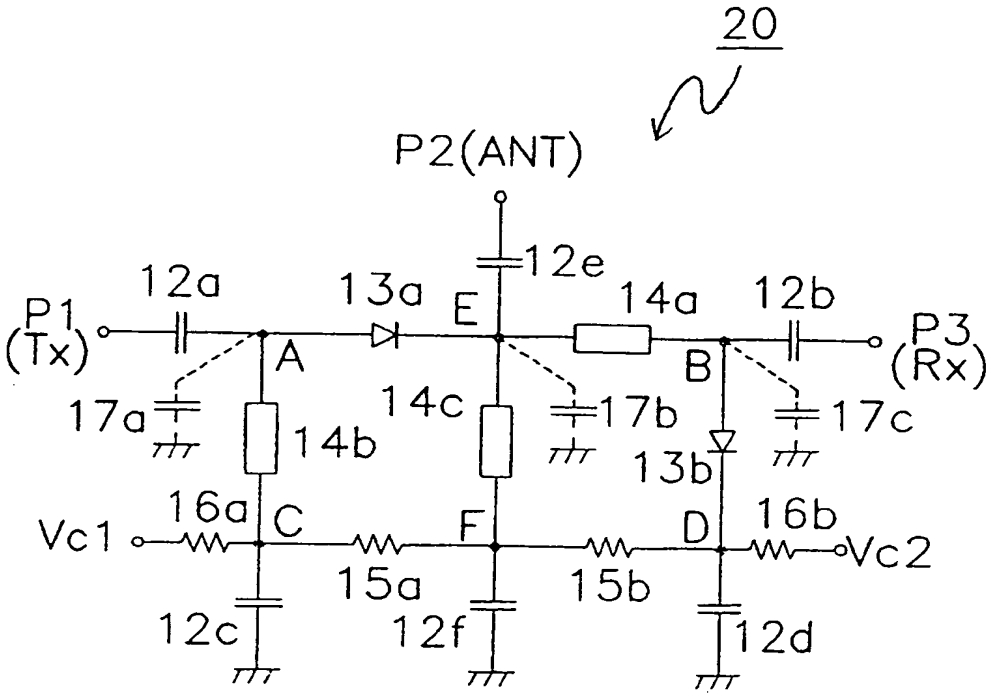


FIG. 4

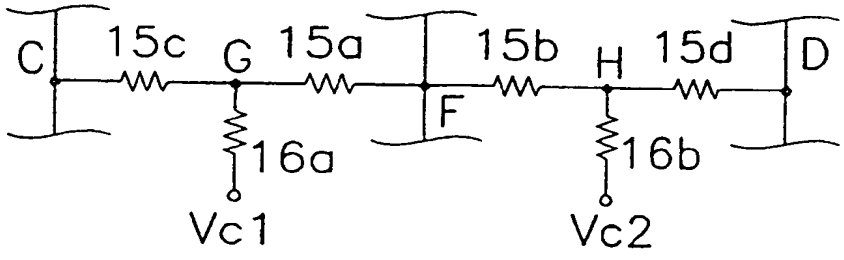


FIG. 5

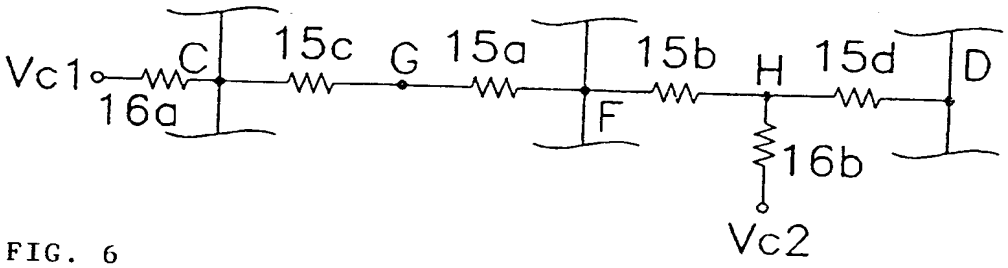


FIG. 6

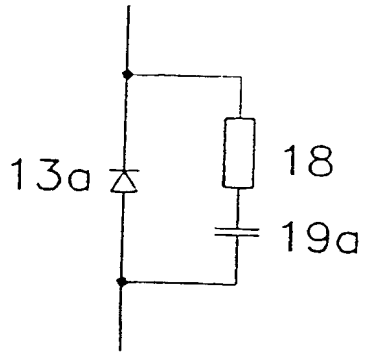


FIG. 7

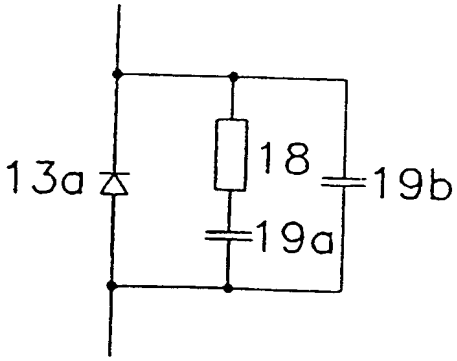


FIG. 8

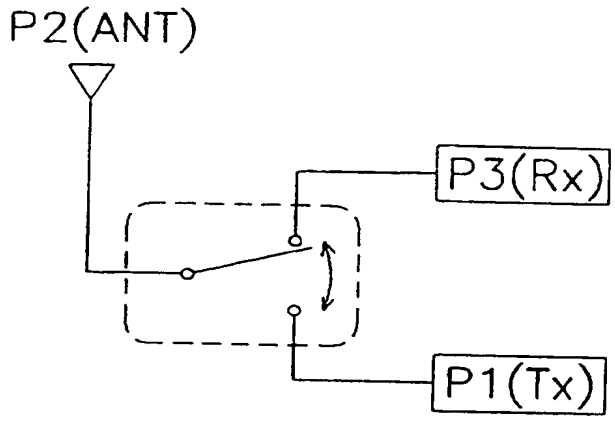


FIG. 9

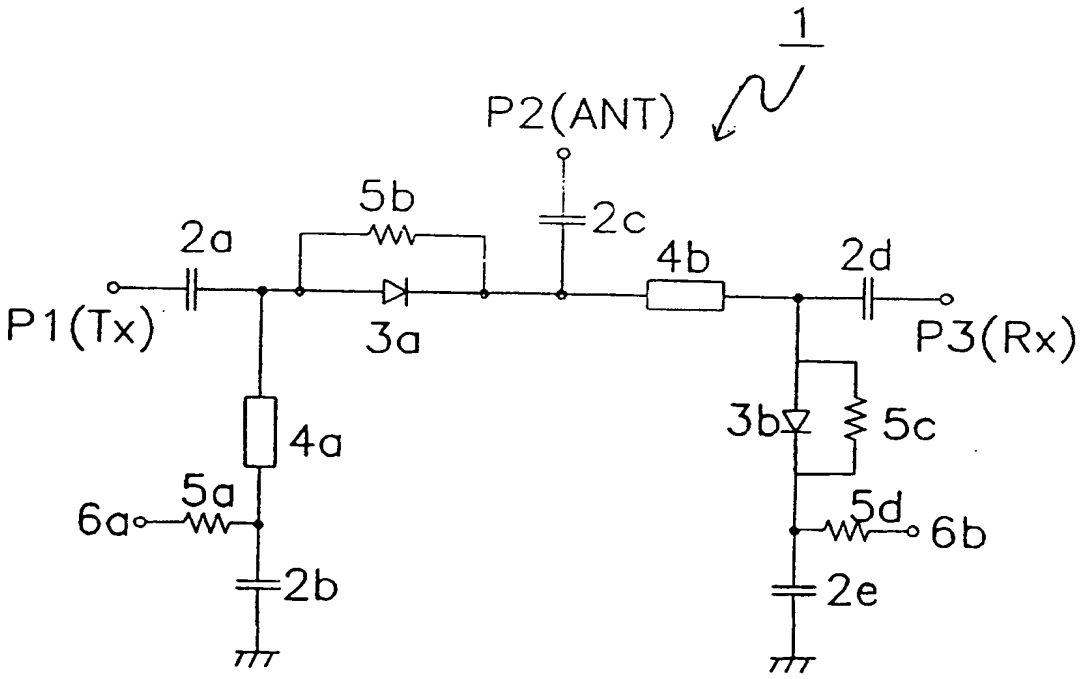


FIG. 10

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## (54) High-frequency switch

(57) A high-frequency switch (10) is disclosed in which required resistors can be mounted without hampering the characteristics of the switch. The high-frequency switch (10) has a series circuit formed of a first diode (13a) and a first transmission line (14a). The first diode (13a) is connected to a transmitting circuit (Tx) through a capacitor. One end of the first transmission line (14a) is coupled to a receiving circuit (Rx) via a capacitor (12b). A second transmission line (14b) and a capacitor (12c) are connected between the node (A) and a ground potential, while a second diode (13b) and a capacitor (12d) are coupled between the node (B) and a ground potential. A series circuit formed of first and second resistors (15a, 15b) is connected between the nodes (C) and (D). A first control voltage terminal (Vc1) is coupled to the node (C) via a resistor (16a), while a second control voltage terminal (Vc2) is connected to the node (D) via another resistor (16b). An antenna (ANT) and the node (E) are connected to the node (F).

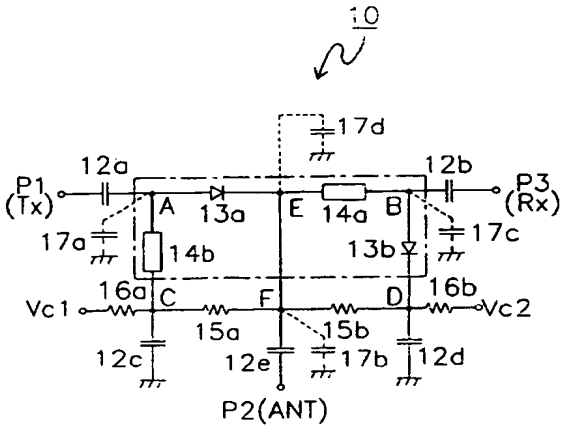


FIG. 1

EP 0 778 671 A3

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number
EP 96 11 9568

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int.Cl.6) |
|---|---|---|---|
| A | GB 2 289 574 A (MURATA MANUFACTURING CO) * page 8, line 6 - page 12; figure 4 * | 1-3,5,6 | H03K17/76 |
| A | DE 43 43 719 A (MURATA MANUFACTURING CO) * page 5, line 41 - page 6, line 17; figures 8-11 * | 1-3,6,7 | |
| A | PATENT ABSTRACTS OF JAPAN vol. 008, no. 074 (E-236), 6 April 1984 & JP 58 222619 A (FUJITSU KK), 24 December 1983, * abstract * | 1-3 | |

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H03K
H01P
H04B
G01S

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| THE HAGUE | 19 December 1997 | Cantarelli, R |

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